ADCS8162 December 2020

ADCS8162 8-Channel DAS with 16-Bit, Bipolar Input, Simultaneous Sampling ADC

1. General Description

- The ADCS8162 is 16-bit, simultaneous sampling, analog-to-digital data acquisition systems (DAS) with 8-channels, respectively. Each part contains analog input clamp protection, a second-order antialiasing filter, a 16-bit charge redistribution successive approximation analog-to- digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.
- The ADCS8162 operate from a single 5 V supply and can accommodate ±10 V and ±5 V true bipolar input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to ±16.5 V. The ADCS8162 has 1 MΩ analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies.
- The ADCS8162 antialiasing filter has a 3 dB cutoff frequency of 43 kHz and provides 46 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the 3 dB bandwidth.

2. Applications

- Power-line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

3. Features and Benefits

- Single-Supply Operation from +2.5V~+5.5V
- 8 simultaneously sampled inputs
- True bipolar analog input ranges: ±10 V, ±5 V
- Single 5 V analog supply and 2.3 V to 5 V VDRIVE
- Analog input clamp protection
- Input buffer with 1 MΩ analog input impedance
- Second-order antialiasing analog filter
- On-chip accurate reference and reference buffer with 5ppm/℃ drift
- 16-bit ADC with 200 kSPS on all channels
- Oversampling capability with digital filter
- Flexible parallel/serial interface PI/QSP/MICROWIR /DSP compatible
- Performance
- 7 kV ESD rating on analog input channels 89 dB SNR, −106 dB THD
- ±0.5 LSB INL, ±0.5 LSB DNL
- Low power: 130 mW Standby mode: 35 mW
- Temperature range: −40°C to +125°C
- 64-lead LQFP package

4. Device Information

PART NUMBER	PACKAGE	BODY SIZE
ADCS8162	LQFP-64	12mm×12mm

*Refer to theOrdering Information for more

5. Typical Schematics and Circuit Diagram

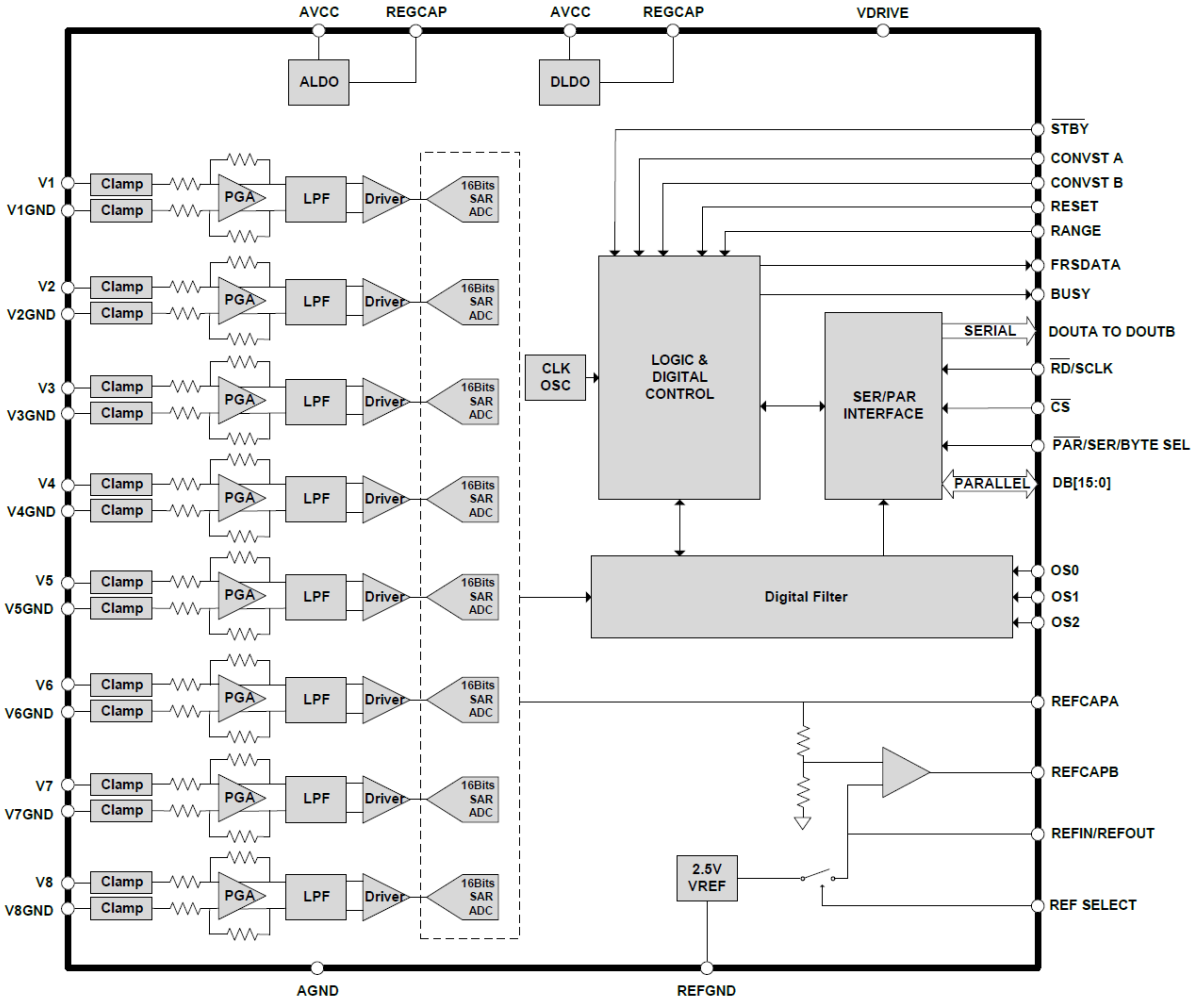

Figure 1 Typical Diagram

CATALOG

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6. Electrical and Magnetic Characteristics

6.1 Absolute maximum ratings

Over operating free-air temperature range

Symbol	Parameter	MIN	MAX	UNIT
AVCC	AVCC to AGND	–0.3	7.0	V
VDRIVE	VDRIVE to DGND	–0.3	7.0	V
	AGND to DGND	–0.3	0.3	V
VAIN	Analog input voltage to AGND	–15	15	V
VD	Digital input to DGND	–0.3	VDRIVE + 0.3	V
Vref	REFIN to AGND	–0.3	AVCC + 0.3	V
Iin	Input current to any pin except supplies	–10	10	mA
TA	Operating Temperature	–40	125	°C
TJ	Junction Temperature, TJ	150		
Tstg	Storage Temperature, Tstg	–65	150	

6.2 ESD Rating

Symbol	Parameter	Conditions		UNIT
VESD-HBM	Human-body model (HBM), per ANSI/ESDA/JEDECJS-001	All pins except analog inputs	±3000	V
		Analog input pins only	±7000	V
VESD-CDM	Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins	±500	V

6.3 Thermal Information

Symbol	Parameters		Units
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top)thermal resistance	7.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W

6.4 Electrical Characteristics

At T_A = -40℃ to 125℃, Vs = 1.65V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE		f_{IN}= 1 kHz sine wave unless otherwise noted				
SNR	Signal-to-Noise Ratio (SNR)	Oversampling by 16; ±10 V range; f_{IN} = 155Hz		94		dB
		Oversampling by 16; ±5 V range; f_{IN} = 155Hz		94		dB

		No oversampling; ±10 V Range		89		dB
		No oversampling; ±5 V range		88.9		dB
SINAD	Signal-to-(Noise + Distortion) (SINAD)	No oversampling; ±10 V range		89		dB
		No oversampling; ±5 V range		88.9		dB
THD	Total Harmonic Distortion (THD)			-106	-95	dB
SFDR	Peak Harmonic or Spurious Noise (SFDR)			-109		dB
IMD	Intermodulation Distortion (IMD)	fa = 1 kHz, fb = 1.1 kHz				
	Second-Order Terms			-110		dB
	Third-Order Terms			-111		dB
	Channel-to-Channel Isolation	fINon unselected channels up to 160 kHz		-105		dB
ANALOG INPUT FILTER						
BW(-3dB)	Full Power Bandwidth	−3 dB, ±10 V range		43		kHz
		−3 dB, ±5 V range		20		kHz
BW(-0.1dB)		−0.1 dB, ±10 V range		10		kHz
		−0.1 dB, ±5 V range		5		kHz
$t_{GROUP\ DELAY}$	$t_{GROUP\ DELAY}$	±10 V range		11		µs
		±5 V range		15		µs
DC ACCURACY						
	Resolution	No missing codes	16			Bits
DNL	Differential Nonlinearity			±0.5	±0.99	LSB
INL	Integral Nonlinearity			±0.5	±2	LSB
TUE	Total Unadjusted Error (TUE)	±10 V range		±6	±15	LSB
		±5 V range		±5	±15	LSB
E_{PFS}	Positive Full-Scale Error	External reference		±5	±20	LSB
		Internal reference		±5		LSB
	Positive Full-Scale Error Drift	External reference		±2		ppm/°C
		Internal reference		±5	±15	ppm/°C

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Positive Full-Scale Error Matching	±10 V range		6	15	LSB
		±5 V range		5	15	LSB
E_{ZC}	Bipolar Zero Code Error	±10 V range		±1	±6	LSB
		± 5 V range		±2	±6	LSB
	Bipolar Zero Code Error Drift	±10 V range		5		µV/°C
		± 5 V range		7.5		µV/°C
	Bipolar Zero Code Error Matching	±10 V range		3	6	LSB
		±5 V range		3	6	LSB
E_{NFS}	Negative Full-Scale Error	External reference		±5	±20	LSB
		Internal reference		±5		LSB
	Negative Full-Scale Error Drift	External reference		±2		ppm/°C
		Internal reference		±5	±15	ppm/°C
	Negative Full-Scale Error Matching	±10 V range		6	15	LSB
		±5 V range		5	15	LSB
ANALOG INPUT						
A_{IN}	Input Voltage Ranges	RANGE = 1			±10	V
		RANGE = 0			±5	V
Iin	Analog Input Current	With voltage at A_{IN} = V_{IN}, all input ranges		(VIN – 2) / RIN		µA
C_{AIN}	Input Capacitance			2		pF
Rin	Input Impedance	See the Analog Input section		1		MΩ
REFERENCE INPUT/OUTPUT						
V_{REF-IN}	Reference Input Voltage Range	See the ADC Transfer Function section	2.475	2.5	2.525	V
I_{RLK}	DC Leakage Current				±1	µA
C_{REFIN}	Input Capacitance	REF SELECT = 1		7.5		pF
$V_{REF-OUT}$	Reference Output Voltage	REFIN/REFOUT	2.49	2.5	2.505	V
	Reference Temperature Coefficient			±5	±15	ppm/°C
LOGIC INPUTS						
V_{INH}	Input High Voltage (V_{INH})		0.7 × V_{DRIVE}			V
V_{INL}	Input Low Voltage (V_{INL})				0.3 × V_{DRIVE}	V
I_{IN}	Input Current (I_{IN})				±2	µA
C_{LIN}	Input Capacitance (C_{IN})			5		pF
LOGIC OUTPUTS						
V_{OH}	Output High Voltage (V_{OH})	I_{SOURCE}= 100 µA	VDRIVE-0.2			V
V_{OL}	Output Low Voltage (V_{OL})	I_{SINK}= 100 µA			0.2	V
I_{LLK}	Floating-State Leakage Current			±1	±20	µA
C_{LOUT}	Floating-State Output Capacitance			5		pF
	Output Coding	Two's complement				

Symbol	Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS						
AVCC	AVCC		4.75		5.25	V
VDRIVE	VDRIVE		2.3		5.25	V
ITOTAL	ITOTAL	Digital inputs = 0 V or VDRIVE				
IStatic	Normal Mode (Static)			8		mA
IAVCC	Normal Mode (Operational)	fSAMPLE=200ksps		26		mA
ISTDBY	Standby Mode			7		mA
ISTDN	Shutdown Mode			6		mA

7. Timing Characteristics

AVCC = 4.75 V to 5.25 V, VDRIVE = 2.3 V to 5.25 V, VREF = 2.5 V external reference/internal reference, TA = TMIN to TMAX, unless otherwise noted.

Symbol	Parameter	Limit at TMIN, TMAX (0.1 × VDRIVE and 0.9 × VDRIVE Logic Input Levels)			Limit at TMIN, TMAX (0.3 ×VDRIVE and 0.7 × VDRIVE Logic Input Levels)			Unit
		Min	Typ	Max	Min	Typ	Max	
PARALLEL/SERIAL/BYTE MODE								
tCYCLE	1/throughput rate							
	Parallel mode, reading during or after conversion; or serial mode: VDRIVE = 3.3 V to 5.25 V, reading during a conversion using DOUTA and DOUTB lines			5			5	µs
	Serial mode reading after a conversion; VDRIVE =2.7 V						9.4	µs
	Serial mode reading after a conversion; VDRIVE =2.3 V, DOUTA and DOUTB lines			9.7			10.7	µs
tCONV	Conversion time							
	Oversampling off	3.45	4	4.2	3.45	4	4.2	µs
	Oversampling by 2	7.87		9.1	7.87		9.1	µs
	Oversampling by 4	16.05		18.8	16.05		18.8	µs
	Oversampling by 8	33		39	33		39	µs
	Oversampling by 16	66		78	66		78	µs
	Oversampling by 32	133		158	133		158	µs
	Oversampling by 64	257		315	257		315	µs
tWAKE-UP STANDBY	STBY rising edge to CONVST x rising edge; power-up time from standby mode			100			100	µs
tWAKE-UP SHUTDOWN								
Internal Reference	STBY rising edge to CONVST x rising edge; power-up time from shutdown mode			30			30	ms
External Reference	STBY rising edge to CONVST x rising edge; power-up time from shutdown mode			13			13	ms
tRESET	RESET high pulse width	50			50			ns
tOS_SETUP	BUSY to OS x pin setup time	20			20			ns
tOS_HOLD	BUSY to OS x pin hold time	20			20			ns

Symbol	Parameter	Limit at T_{MIN}, T_{MAX} (0.1 × V_{DRIVE} and 0.9 × VDRIVE Logic Input Levels)			Limit at T_{MIN}, T_{MAX} (0.3 ×VDRIVE and 0.7 × VDRIVE Logic Input Levels)			Unit
		Min	Typ	Max	Min	Typ	Max	
t1	CONVST x high to BUSY high			40			45	ns
t2	Minimum CONVST x low pulse	25			25			ns
t3	Minimum CONVST x high pulse	25			25			ns
t4	BUSY falling edge to CS falling edge setup time	0			0			ns
t5	Maximum delay allowed between CONVST A, CONVST B rising edges			0.5			0.5	ms
t6	Maximum time between last CS rising edge and BUSY falling edge			25			25	ns
t7	Minimum delay between RESET low to CONVST x high	25			25			ns
PARALLEL/BYTE READ OPERATION								
t8	CS to RD setup time	0			0			ns
t9	CS to RD hold time	0			0			ns
t10	RD low pulse width							
	V_{DRIVE} above 4.75 V	16			19			ns
	V_{DRIVE} above 3.3 V	21			24			ns
	V_{DRIVE} above 2.7 V	25			30			ns
	V_{DRIVE} above 2.3 V	32			37			ns
t11	RD high pulse width	15			15			ns
t12	CS high pulse width CS and RD linked	22			22			ns
t13	Delay from CS until DB[15:0] three-state disabled							
	VDRIVE above 4.75 V			16			19	ns
	VDRIVE above 3.3 V			20			24	ns
	VDRIVE above 2.7 V			25			30	ns
	VDRIVE above 2.3 V			30			37	ns
t14	Data access time after RD falling edge							
	VDRIVE above 4.75 V			16			19	ns
	VDRIVE above 3.3 V			21			24	ns
	VDRIVE above 2.7 V			25			30	ns
	VDRIVE above 2.3 V			32			37	ns
t15	Data hold time after RD falling edge	6			6			ns
t16	CS to DB[15:0] hold time	6			6			ns
t17	Delay from CS rising edge to DB[15:0] three- state enabled			22			22	ns
SERIAL READ OPERATION								
f_{SCLK}	Frequency of serial read clock							
	V_{DRIVE} above 4.75 V			23.5			20	MHz
	V_{DRIVE} above 3.3 V			17			15	MHz
	V_{DRIVE} above 2.7 V			14.5			12.5	MHz
	V_{DRIVE} above 2.3 V			11.5			10	MHz
t18	Delay from CS until DOUTA/DOUTB three-state disabled/delay from CS until MSB valid							
	V_{DRIVE} above 4.75 V			15			18	ns

Symbol	Parameter	Limit at T_{MIN}, T_{MAX} (0.1 × V_{DRIVE} and 0.9 × VDRIVE Logic Input Levels)			Limit at T_{MIN}, T_{MAX} (0.3 ×VDRIVE and 0.7 × VDRIVE Logic Input Levels)			Unit
		Min	Typ	Max	Min	Typ	Max	
	V_{DRIVE} above 3.3 V			20			23	ns
	V_{DRIVE} = 2.3 V to 2.7 V			30			35	ns
t19	Data access time after SCLK rising edge							
	V_{DRIVE} above 4.75 V			17			20	ns
	V_{DRIVE} above 3.3 V			23			26	ns
	V_{DRIVE} above 2.7 V			27			32	ns
	V_{DRIVE} above 2.7 V	25			30			ns
	V_{DRIVE} above 2.3 V			34			39	ns
t20	SCLK low pulse width	0.4 t_{SCLK}			0.4 t_{SCLK}			ns
t21	SCLK high pulse width	0.4 t_{SCLK}			0.4 t_{SCLK}			ns
t22	SCLK rising edge to DOUTA/DOUTB valid hold time	7			7			
t23	CS rising edge to DOUTA/DOUTB three-state enabled			22			22	ns
FRSTDATA OPERATION								
t24	Delay from CS falling edge until FRSTDATA three-state disabled							
	V_{DRIVE} above 4.75 V			15			18	ns
	V_{DRIVE} above 3.3 V			20			23	ns
	V_{DRIVE} above 2.7 V			25			30	ns
	V_{DRIVE} above 2.3 V			30			35	ns
t25	Delay from CS falling edge until FRSTDATA high, serial mode							ns
	V_{DRIVE} above 4.75 V			15			18	ns
	V_{DRIVE} above 3.3 V			20			23	ns
	V_{DRIVE} above 2.7 V			25			30	ns
	V_{DRIVE} above 2.3 V			30			35	ns
t26	Delay from RD falling edge to FRSTDATA high							
	V_{DRIVE} above 4.75 V			16			19	ns
	V_{DRIVE} above 3.3 V			20			23	ns
	V_{DRIVE} above 2.7 V			25			30	ns
	V_{DRIVE} above 2.3 V			30			35	ns
t27	Delay from RD falling edge to FRSTDATA low							
	V_{DRIVE} = 3.3 V to 5.25V			19			22	ns
	V_{DRIVE} = 2.3 V to 2.7V			24			29	ns
t28	Delay from 16th SCLK falling edge to FRSTDATA low							
	V_{DRIVE} = 3.3 V to 5.25V			17			20	ns
	V_{DRIVE} = 2.3 V to 2.7V			22			27	ns
t29	Delay from CS rising edge until FRSTDATA three-state enabled			24			29	ns

8. Timing Diagram

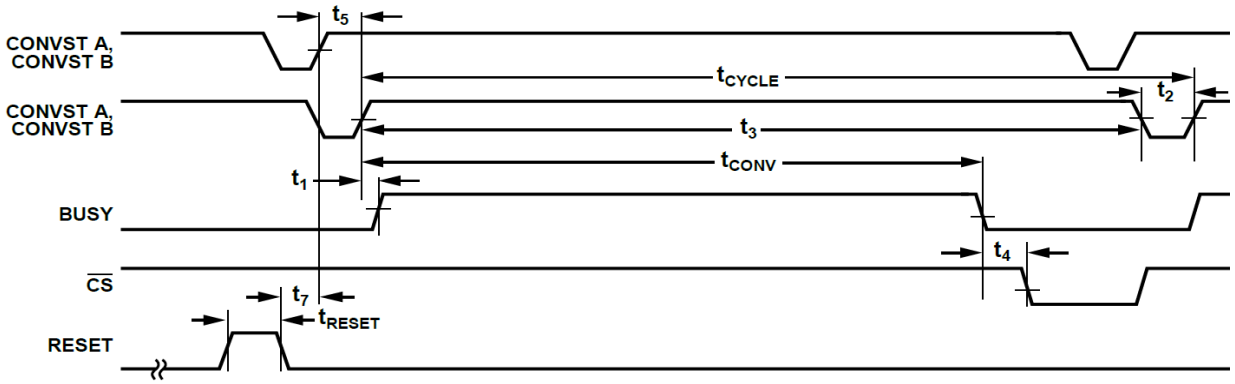


Figure 2 CONVST Timing—Reading After a Conversion

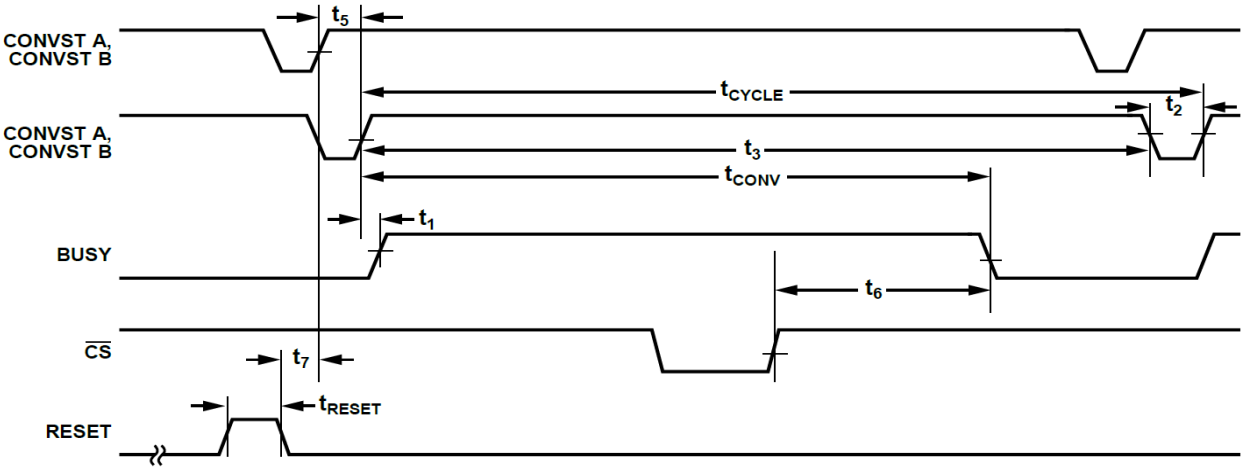


Figure 3. CONVST Timing—Reading During a Conversion

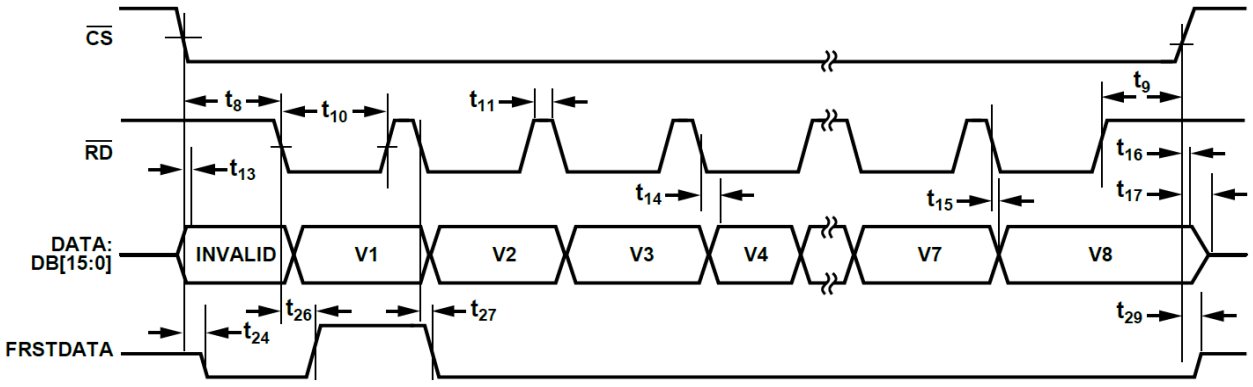


Figure 4. Parallel Mode, Separate CS and RD Pulses

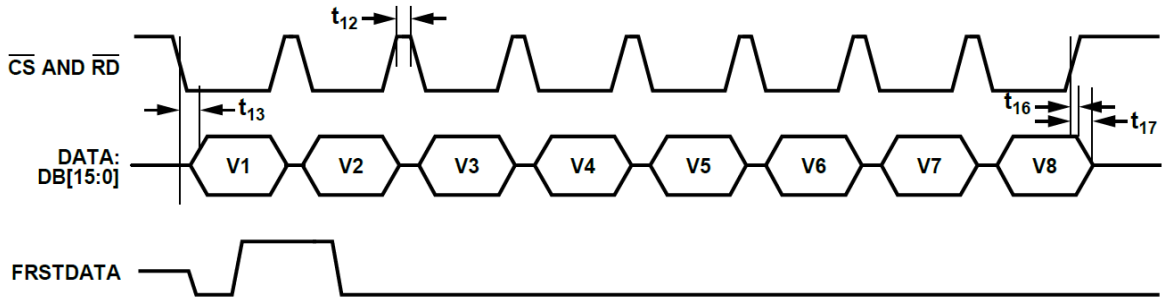


Figure 5. CS and RD, Linked Parallel Mode

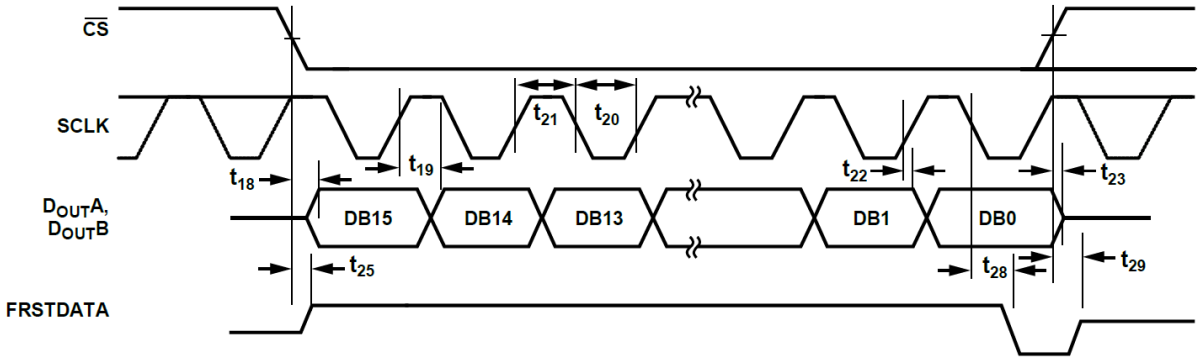


Figure 6. Serial Read Operation (Channel 1)

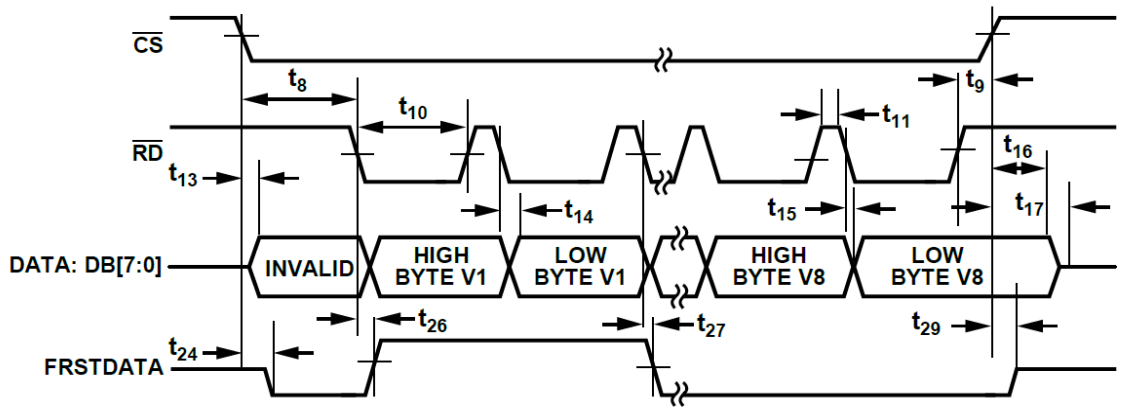


Figure 7. BYTE Mode Read Operation

9. PIN Configuration

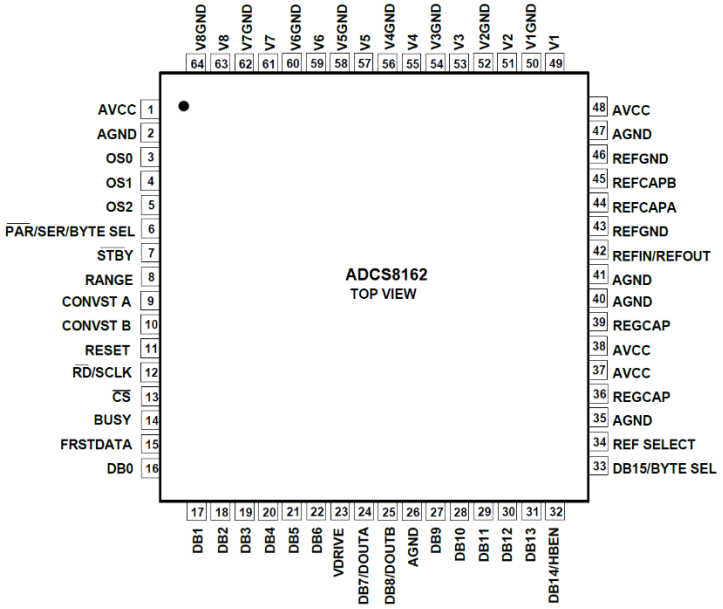


Figure8 PIN configuration

Table 1. Pin functions

PIN		TYPE	DESCRIPTION
Name	NO.		
AGND	2, 26, 35, 40, 41, 47	P	Analog ground pins
V1GND	50	AI	Analog input channel 1: negative input
V1P	49	AI	Analog input channel 1: positive input
V2GND	52	AI	Analog input channel 2: negative input
V2P	51	AI	Analog input channel 2: positive input
V3GND	54	AI	Analog input channel 3: negative input
V3P	53	AI	Analog input channel 3: positive input
V4GND	56	AI	Analog input channel 4: negative input
V4P	55	AI	Analog input channel 4: positive input
V5GND	58	AI	Analog input channel 5: negative input
V5P	57	AI	Analog input channel 5: positive input
V6GND	60	AI	Analog input channel 6: negative input
V6P	59	AI	Analog input channel 6: positive input
V7GND	62	AI	Analog input channel 7: negative input
V7P	61	AI	Analog input channel 7: positive input
V8GND	64	AI	Analog input channel 8: negative input
V8P	63	AI	Analog input channel 8: positive input
AVCC	1, 37, 38, 48	P	Analog supply pins. Decouple these pins to the closest AGND pins
BUSY	14	DO	Active high digital output indicating ongoing conversion
CONVSTA	9	DI	Active high logic input to control start of conversion for first half count of device input channels

CONVSTB	10	DI	Active high logic input to control start of conversion for second half count of device input channels
$\overline{CS}$	13	DI	Active low logic input chip-select signal
DB0	16	DO	Data output DB0 (LSB) in parallel interface mode
DB1	17	DO	Data output DB1 in parallel interface mode
DB2	18	DO	Data output DB2 in parallel interface mode
DB3	19	DO	Data output DB3 in parallel interface mode
DB4	20	DO	Data output DB4 in parallel interface mode
DB5	21	DO	Data output DB5 in parallel interface mode
DB6	22	DO	Data output DB6 in parallel interface mode
DB7/DOUTA	24	DO	Multi-function logic output pin; this pin is data output DB7 in parallel and parallel byte interface mode; this pin is a data output pin in serial interface mode.
DB8/DOUTB	25	DO	Multi-function logic output pin; this pin is data output DB8 in parallel interface mode; this pin is a data output pin in serial interface mode.
DB9	27	DO	Data output DB9 in parallel interface mode
DB10	28	DO	Data output DB10 in parallel interface mode
DB11	29	DO	Data output DB11 in parallel interface mode
DB12	30	DO	Data output DB12 in parallel interface mode
DB13	31	DO	Data output DB13 in parallel interface mode
DB14/HBEN	32	DIO	Multi-function logic input or output pin: this pin is data output DB14 in parallel interface mode; this pin is a control input pin for byte selection (high or low) in parallel byte interface mode
DB15/BYTE SEL	33	DIO	Multi-function logic input or output pin: this pin is data output DB15 (MSB) in parallel interface mode; this pin is an active high control input pin to enable parallel byte interface mode.
VDRIVE	23	P	Digital supply pin; decouple with AGND on pin 26.
FRSTDATA	15	DO	Active high digital output indicating data read back from channel 1 of the device
OS0	3	DI	Oversampling mode control pin
OS1	4	DI	Oversampling mode control pin
OS2	5	DI	Oversampling mode control pin
PAR/SER /BYTE SEL	6	DI	Logic input pin to select between parallel, serial, or parallel byte interface mode
RANGE	8	DI	Multi-function logic input pin: when STBY pin is high, this pin selects the input range of the device (±10 V or ±5 V); when STBY pin is low, this pin selects between the standby and shutdown modes.
$\overline{RD}$/SCLK	12	DI	Multi-function logic input pin: this pin is an active-low ready input pin in parallel and parallel byte interface; this pin is a clock input pin in serial interface mode.
REFCAPA	44	AO	Reference amplifier output pins. This pin must be shorted to REFCAPB and decoupled to AGND using a low ESR, 10-µF ceramic capacitor.
REFCAPB	45	AO	Reference amplifier output pins. This pin must be shorted to REFCAPA and decoupled to AGND using a low ESR, 10-µF ceramic capacitor.
REFGND	43, 46	P	Reference GND pin. This pin must be shorted to the analog GND plane and decoupled with REFIN/REFOUT on pin 42 using a 10-µF capacitor.
REFIN/REFOUT	42	AIO	This pin acts as an internal reference output when REFSEL is high; this pin functions as input pin for the external reference when REFSEL is low; decouple with REFGND on pin 43 using a 10-µF capacitor.
REFSEL	34	DI	Active high logic input to enable the internal reference
REGCAP1	36	AO	Output pin 1 for the internal voltage regulator; decouple separately to AGND using a 1-µF capacitor.
REGCAP2	39	AO	Output pin 2 for the internal voltage regulator; decouple separately to AGND using a 1-µF capacitor.
RESET	11	DI	Active high logic input to reset the device digital logic

$\overline{\text{STBY}}$	7	DI	Active low logic input to enter the device into one of the two power-down modes: standby or shutdown

10. Detailed Description

10.1 CONVERTER DETAILS

The ADCS8162 are data acquisition systems that employ a high speed, low power, charge redistribution, successive approximation analog-to-digital converter (ADC) and allow the simultaneous sampling of eight analog input channels. The analog inputs on the ADCS8162can accept true bipolar input signals. The RANGE pin is used to select either ±10 V or ±5 V as the input range.

The ADCS8162 operate from a single 5 V supply. The ADCS8162 contain input clamp protection, input signal scaling amplifiers, a second-order anti- aliasing filter, an on-chip reference, reference buffers, a highspeed ADC, a digital filter, and high speed parallel and serial interfaces. Sampling on the ADCS8162 is controlled using the CONVST signals.

10.2 ANALOG INPUT

Analog Input Ranges

The ADCS8162 can handle true bipolar, single-ended input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range; however, there is typically a settling time of approximately 80 µs, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the RANGE pin according to the desired input range for the system signals.

During normal operation, the applied analog input voltage should remain within the analog input range selected via the RANGE pin. A RESET pulse must be applied after power up to ensure the analog input channels are configured for the range selected.

When in a power-down mode, it is recommended to tie the analog inputs to GND. Per the Analog Input ClampProtection section, the overvoltage clamp protection is recommended for use in transient overvoltage conditions and should not remain active for extended periods. Stressing the analog inputs outside of the conditions mentioned here may degrade the bipolar zero code error and THD performance of the ADCS8162.

Analog Input Impedance

The analog input impedance of the ADCS8162 is 1 MΩ. This is a fixed input impedance that does not vary with the AD~~CS~~8162 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the ADCS8162, allowing for direct connection to the source or sensor. With the need for a driver amplifier eliminated, bipolar supplies (which are often a source of noise in a system) can be removed from the signal chain.

Analog Input Clamp Protection

Figure9 shows the analog input structure of the ADCS8162.Each analog input of the ADCS8162 contains clamp protection circuitry. Despite single 5 V supply operation, this analog input clamp protection allows for an input over voltage of up to ±16.5V.

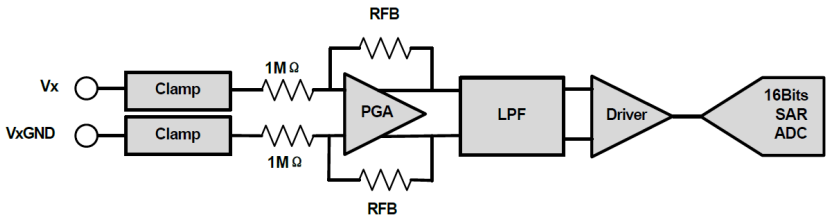


Figure 9 Analog input

Figure 10 shows the voltage vs. current characteristic of the clamp circuit. For input voltages of up to ±16.5 V, no current flows in the clamp circuit. For input voltages that are above ±16.5 V, the ADCS8162 clamp circuitry turns on.

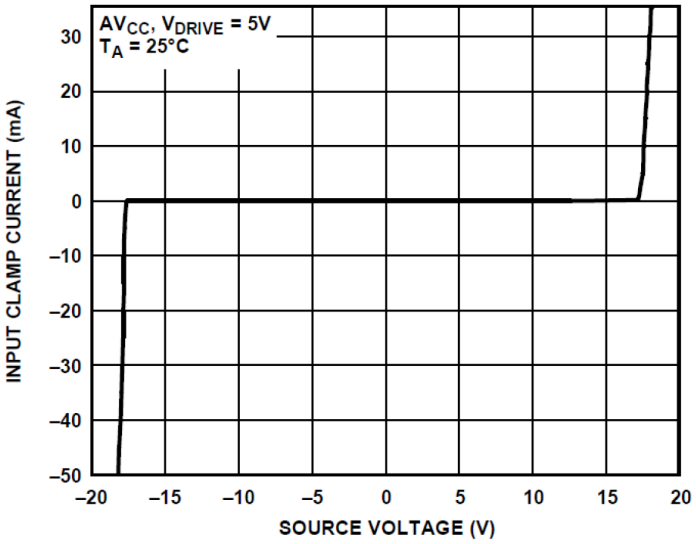


Figure 10 Clamp circuit characteristic

A series resistor should be placed on the analog input channels to limit the current to ±10 mA for input voltages above ±16.5V. In an application where there is a series resistance on an analog input channel, Vx, a corresponding resistance is required on the analog input GND channel, VxGND (see Figure 11). If there is no corresponding resistor on the VxGND channel, an offset error occurs on that channel. It is recommended that the input overvoltage clamp protection circuitry be used to protect the ADCS8162 against transient overvoltage events. It is not recommended to leave the ADCS8162 in a condition where the clamp protection circuitry is active in normal or power-down conditions for extended periods because this may degrade the bipolar zero code error performance of the ADCS8162.

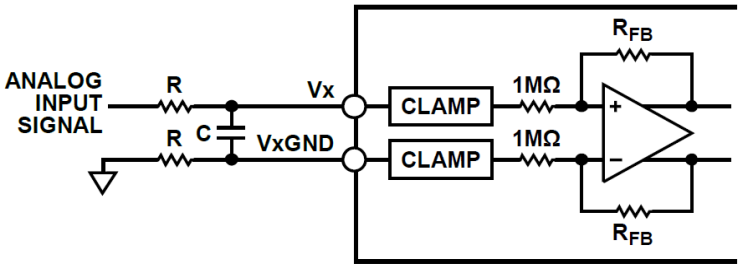


Figure 11 Input Resistance Matching on the Analog Input

Analog Input Antialiasing Filter

An analog antialiasing filter is also provided on the ADCS8162. In the ±5 V range, the −3 dB frequency is typically 15 kHz. In the ±10 V range, the −3 dB frequency is typically 23 kHz.

10.3 ADC TRANSFER FUNCTION

The output coding of the ADCS8162 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is FSR/65, 536 for the ADCS8162. The ideal transfer characteristic for the ADCS8162 is shown in Figure 12. The LSB size is dependent on the analog input range selected.

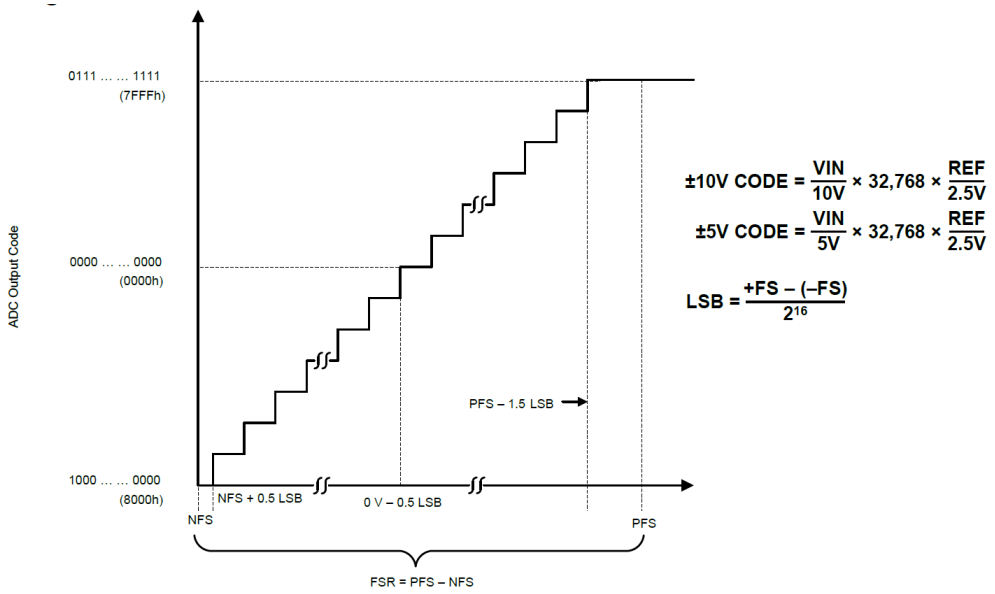


Figure 12 Transfer Characteristics

	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	305μV
±5V RANGE	+5V	0V	–5V	152μV

10.4 INTERNAL/EXTERNAL REFERENCE

The ADCS8162 contain an on-chip 2.5 V band gap reference. The REFIN/REFOUT pin allows access to the2.5V reference that generates the on-chip 4.0 V reference internally, or it allows an external reference of 2.5 V to be applied to the ADCS8162. An externally applied reference of 2.5 V is also gained up to 4.0 V, using the internal buffer. This 4.0 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the ADCS8162 operate in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal and external reference options. A 10 μF ceramic capacitor is required on the REFIN/REFOUT pin.

The ADCS8162 contain a reference buffer configured to gain the REF voltage up to ~4.0 V, as shown in Figure13. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 μF applied to REFGND, to ensure that the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

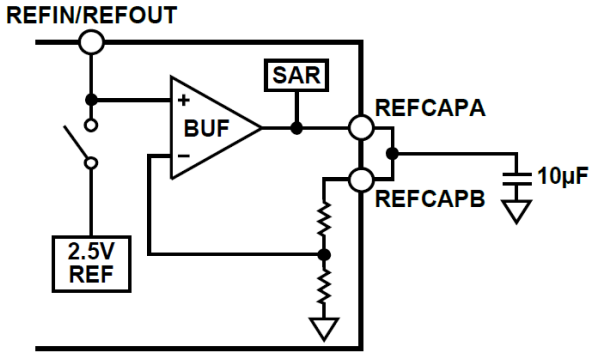


Figure 13 Reference Circuitry

When the ADCS8162 are configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple ADCS8162 devices, the following configurations are recommended, depending on the application requirements.

External Reference Mode

One external reference can be used to drive the REFIN/REFOUT pins of one or multi-chip ADCS8162 devices. In this configuration, each REFIN/REFOUT pin of the ADCS8162 should be decoupled with at least a 100 nF decoupling capacitor.

Internal Reference Mode

One ADCS8162 device, configured to operate in the internal reference mode, can be used to drive the remaining ADCS8162 devices, which are configured to operate in external reference mode. The REFIN/ REFOUT pin of the ADCS8162, configured in internal reference mode, should be decoupled using a 10 µF ceramic decoupling capacitor. The other ADCS8162 devices, configured in external reference mode, should use at least a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

10.5 TYPICAL CONNECTION DIAGRAM

Figure 14 shows the typical connection diagram for the ADCS8162. There are four AVCC supply pins on the part, and each of the four pins should be decoupled using a 100 nF capacitor at each supply pin and a 10 µF capacitor at the supply source. The ADCS8162 can operate with the internal reference or an externally applied reference. In this configuration, the ADCS8162 is configured to operate with the internal reference. When using a single ADCS8162 device on the board, the REFIN/REFOUT pin should be decoupled with a 10 µF capacitor. Refer to the Internal/External Reference section when using an application with multiple ADCS8162 devices. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.
The VDRIVE supply is connected to the same supply as the processor. The VDRIVE voltage controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.
After supplies are applied to the ADCS8162, a reset should be applied to the ADCS8162 to ensure that it is configured for the correct mode of operation.

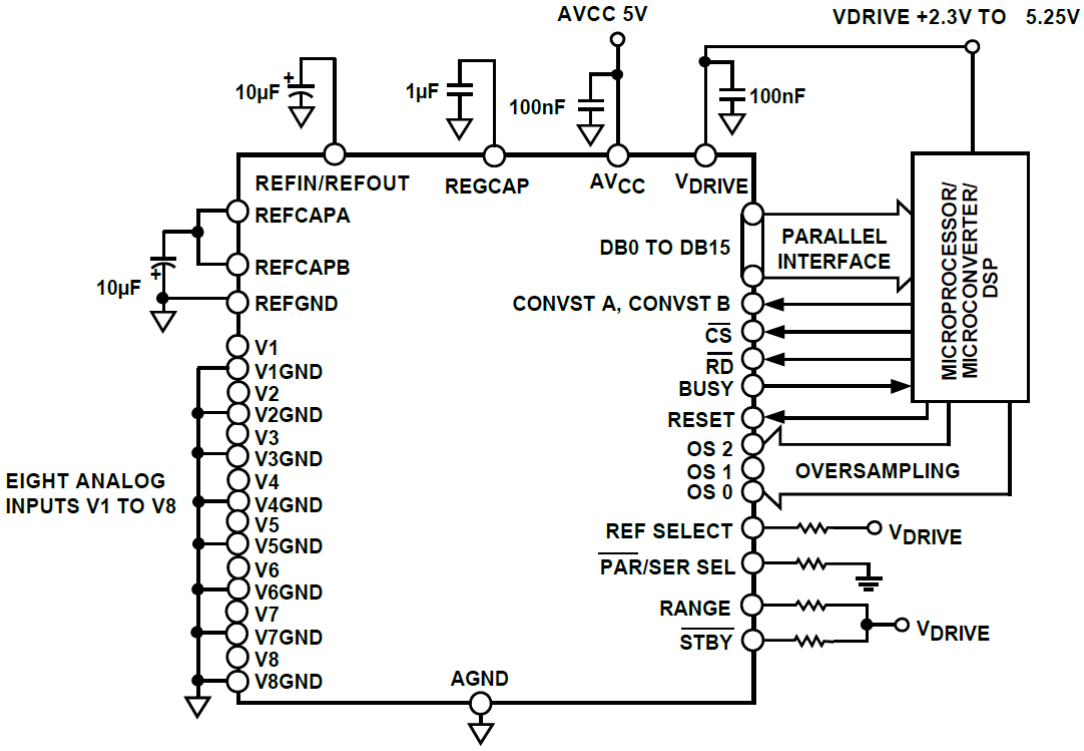


Figure 14 Typical Connection Diagram

10.6 POWER-DOWN MODES

Two power-down modes are available on the ADCS8162: standby mode and shutdown mode. The STBY pin controls whether the ADCS8162 are in normal mode or in one of the two power-down modes.

The power-down mode is selected through the state of the RANGE pin when the STBY pin is low. Table 6 shows the configurations required to choose the desired power-down mode. When the ADCS8162 are placed in standby mode, the current consumption is 7 mA maximum and power- up time is approximately 100 µs because the capacitor on the REFCAPA and REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up, and the amplifiers and ADC core are powered down.

Table 6. Power-Down Mode Selection

Power-Down Mode	STBY	RANGE
Standby	0	1
Shutdown	0	0

When the ADCS8162 are placed in shutdown mode, the current consumption is 6 mA maximum and power-up time is approximately 13 ms (external reference mode). In shut- down mode, all circuitry is powered down. When the ADCS8162 are powered up from shutdown mode, a RESET signal must be applied to the ADCS8162 after the required power-up time has elapsed.

10.7 CONVERSION CONTROL

Simultaneous Sampling on All Analog Input Channels

The ADCS8162 allow simultaneous sampling of all analog input channels. All channels are sampled simul- taneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both CONVST x inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all analog input channels (V1 to V8 for the ADCS8162).

The ADCS8162 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels is tCONV. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge

of CONVST is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB[15:0]), the DOUTA and DOUTB serial data lines, or the parallel byte bus, DB[7:0].

Simultaneously Sampling Two Sets of Channels

The ADCS8162 also allow the analog input channels to be sampled simultaneously in two sets. This can be used in power-line protection and measurement systems to compensate for phase differences introduced by PT and CT transformers. In a 50 Hz system, this allows for up to 9° of phase compensation; and in a 60 Hz system, it allows for up to 10° of phase compensation.
This is accomplished by pulsing the two CONVST pins independently and is possible only if oversampling is not in use. CONVST A is used to initiate simultaneous sampling of the first set of channels (V1 to V4 for the ADCS8162); and CONVST B is used to initiate simultaneous sampling on the second set of analog input channels (V5 to V8 for the ADCS8162), as illustrated in Figure 15. The conversion process begins once both rising edges of CONVST x have occurred; therefore BUSY goes high on the rising edge of the later CONVST x signal. In Table 3, Time t5 indicates the maximum allowable time between CONVST x sampling points.

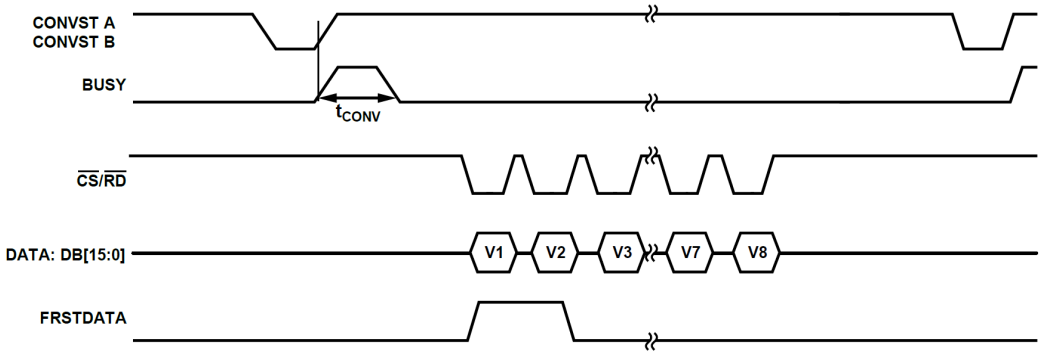


Figure 15 Simultaneous Sampling on Channel Sets While Using Independent CONVST A and CONVST B Signals—Parallel Mode

There is no change to the data read process when using two separate CONVST x signals. Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

10.8 DIGITAL INTERFACE

The ADCS8162 provide three interface options: a parallel interface, a high speed serial interface, and a parallel byte interface. The required interface mode is selected via the PAR/SER/BYTE SEL and DB15/BYTE SEL pins.

Table 7. Interface Mode Selection

PAR/SER/BYTE SEL	DB15	Interface Mode
0	0	Parallel interface mode
1	0	Serial interface mode
1	1	Parallel byte interface mode

PARALLELINTERFACE(PAR/SER/BYTESEL=0)

Data can be read from the ADCS8162via the parallel data bus with standard CS and RD signals. To read the data over the parallel bus, the PAR/SER/BYTE SEL pin should be tied low. The CS and RD input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both CS and RD are logic low.

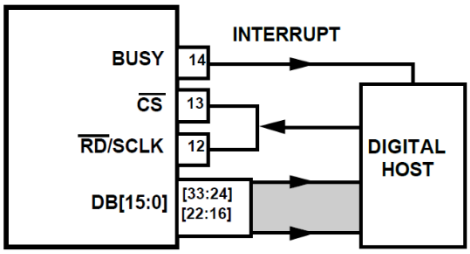


Figure 16 ADCS8162 Interface Diagram—Parallel Bus, with CS and RD Shorted Together

The rising edge of the CS input signal three-states the bus, and the falling edge of the CS input signal takes the bus out of the high impedance state. CS is the control signal that enables the data lines; it is the function that allows multiple ADCS8162 devices to share the same parallel data bus.The CS signal can be permanently tied low, and the RD signal can be used to access the conversion results as shown in Figure 5. A read operation of new data can take place after the BUSY signal goes low (see Figure 2); or, alternatively, a read operation of data from the previous conversion process can take place while BUSY is high (see Figure 3).The RD pin is used to read data from the output conversion results register. Applying a sequence of RD pulses to the RD pin of the ADCS8162 clocks the conversion results out from each channel onto the Parallel Bus DB[15:0] in ascending order. The first RD falling edge after BUSY goes low clocks out the conversion result from Channel V1. The next RD falling edge updates the bus with the V2 conversion result, and so on. On the ADCS8162, the eighth falling edge of RD clocks out the conversion result for Channel V8.

When the RD signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).When there is only one ADCS8162 in a system/board and it does not share the parallel bus, data can be read using just one control signal from the digital host. The CS and RD signals can be tied together, as shown in Figure 6.In this case, the data bus comes out of three-state on the falling edge of CS/RD. The combined CS and RD signal allows the data to be clocked out of the ADCS8162 and to be read by the digital host. In this case, CS is used to frame the data transfer of each data channel.

PARALLEL BYTE (PAR/SER/BYTE SEL = 1, DB15 = 1)

Parallel byte interface mode operates much like the parallel interface mode, except that each channel conversion result is read out in two 8-bit transfers. Therefore, 16 RD pulses are required to read all eight conversion results from the ADCS8162.To configure the ADCS8162 to operate in parallel byte mode, the PAR/SER/BYTE SEL and BYTE SEL/DB15 pins should be tied to logic high (see Table 7). In parallel byte mode, DB[7:0] are used to transfer the data to the digital host. DB0 is the LSB of the data transfer, and DB7 is the MSB of the data transfer. In parallel byte mode, DB14 acts as an HBEN pin. When DB14/HBEN is tied to logic high, the most significant byte (MSB) of the conversion result is output first, followed by the LSB of the conversion result. When DB14 is tied to logic low, the LSB of the conversion result is output first, followed by the MSB of the conversion result. The FRSTDATA pin remains high until the entire 16 bits of the conversion result from V1 are read from the ADCS8162.

SERIAL INTERFACE (PAR/SER/BYTE SEL = 1)

To read data back from the ADCS8162 over the serial interface, the PAR/SER/BYTE SEL pin must be tied high. The CS and SCLK signals are used to transfer data from the ADCS8162. The ADCS8162 have two serial data output pins, DOUTA and DOUTB. Data can be read back from the ADCS8162 using one or both of these DOUT lines. For the ADCS8162, conversion results from Channel V1 to Channel V4 first appear on DOUTA, and conversion results from Channel V5 to Channel V8 first appear on DOUTB.The CS falling edge takes the data output lines, DOUTA and DOUTB, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, DOUTA and DOUTB. The CS input can be held low for the entire serial read operation,

or it can be pulsed to frame each channel read of 16 SCLK cycles. Figure 17 shows a read of eight simultaneous conversion results using two DOUT lines on the ADCS8162.

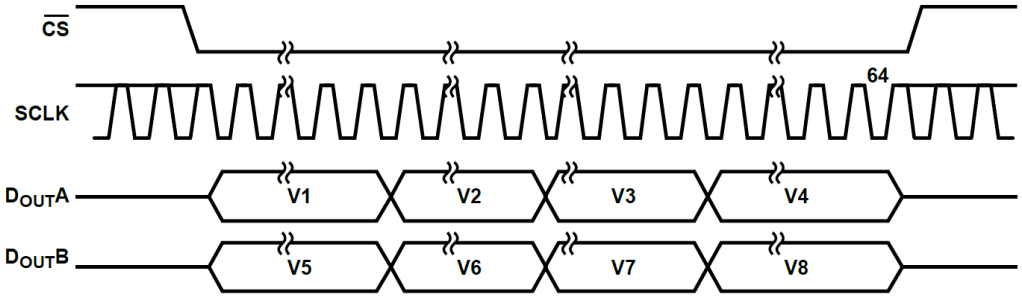


Figure 17. ADCS8162 Serial Interface with Two DOUT Lines

In this case, a 64 SCLK transfer is used to access data from the ADCS8162, and CS is held low to frame the entire 64 SCLK cycles. Data can also be clocked out using just one DOUT line, in which case it is recommended that DOUTA be used to access all conversion data because the channel data is output in ascending order. For the ADCS8162 to access all eight conversion results on one DOUT line, a total of 128 SCLK cycles is required. These 128 SCLK cycles can be framed by one CS signal, or each group of 16 SCLK cycles can be individually framed by the CS signal. The disadvantage of using just one DOUT line is that the throughput rate is reduced if reading occurs after conversion. The unused DOUT line should be left unconnected in serial mode.For the ADCS8162, if DOUTB is to be used as a single DOUT line, the channel results are output in the following order: V5, V6, V7, V8, V1, V2, V3, and V4; however, the FRSTDATA indicator returns low after V5 is read on DOUTB.Figure 7 shows the timing diagram for reading one channel of data, framed by the CS signal, from the ADCS8162 in serial mode. The SCLK input signal provides the clock source for the serial read operation. The CS goes low to access the data from the ADCS8162.The falling edge of CS takes the bus out of three-state and clocks out the MSB of the 16-bit conversion result. This MSB is valid on the first falling edge of the SCLK after the CS falling edge. The subsequent 15 data bits are clocked out of the ADCS8162 on the SCLK rising edge. Data is valid on the SCLK falling edge. To access each conversion result, 16 clock cycles must be provided to the ADCS8162.The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the CS input is high, the FRSTDATA output pin is in three-state. In serial mode, the falling edge of CS takes FRSTDATA out of three- state and sets the FRSTDATA pin high, indicating that the result from V1 is available on the DOUTA output data line. The FRSTDATA output returns to a logic low following the 16th SCLK falling edge. If all channels are read on DOUTB, the FRSTDATA output does not go high when V1 is being output on this serial data output pin. It goes high only when V1 is available on DOUTA (and this is when V5 is available on DOUTB for the ADCS8162).

10.9 READING DURING CONVERSION

Data can be read from the ADCS8162 while BUSY is high and the conversions are in progress. This has little effect on the performance of the converter, and it allows a faster throughput rate to be achieved. A parallel, parallel byte, or serial read can be performed during conversions and when oversampling may or may not be in use. Figure 3 shows the timing diagram for reading while BUSY is high in parallel or serial mode. Reading during conversions allows the full throughput rate to be achieved when using the serial interface with VDRIVE above 4.75 V.Data can be read from the ADCS8162 at any time other than on the falling edge of BUSY because this is when the output data registers are updated with the new conversion data. Time t6, should be observed in this condition.

10.10 DIGITAL FILTER

The ADCS8162 contain an optional digital first-order sinc filter that should be used in applications where slower throughput rates are used or where higher signal-to-noise ratio or dynamic range is desirable. The oversampling ratio of the digital filter is controlled using the oversampling pins, OS [2:0] (see Table 1). OS 2 is the MSB control bit, and OS 0 is the LSB control bit. Table 8 provides the oversampling bit decoding to select the different oversample rates.

The OS pins are latched on the falling edge of BUSY. This sets the oversampling rate for the next conversion (see Figure 46). In addition to the oversampling function, the output result is decimated to 16-bit resolution.

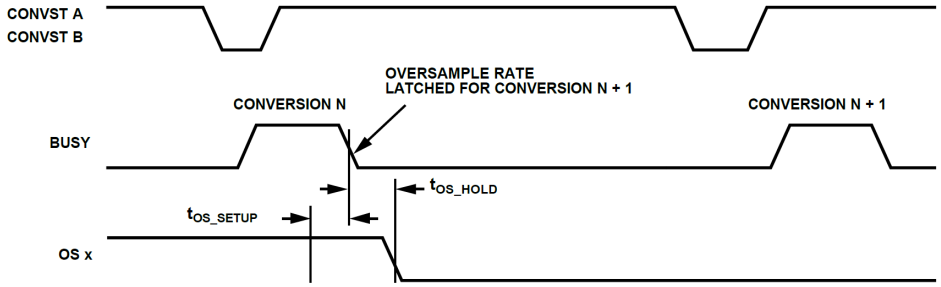


Figure 18 OS x Pin Timing

Table 1. Oversample Bit Decoding

OS[2:0]	OS Ratio	SNR 5 V Range (dB)	SNR 10 V Range (dB)	3 dB BW 5V Range(kHz)	3 dB BW 10 V Range (kHz)	Maximum Throughput CONVST Frequency (kHz)
000	No OS	88.5	89	20	43	200
001	2	90.3	91	15	22	100
010	4	91.7	92.5	13.7	18.5	50
011	8	93.2	93.4	10.3	11.9	25
100	16	94.8	95	6	6	12.5
101	32	95.1	95.6	3	3	6.25
110	64	95.8	96.1	1.5	1.5	3.125
111	Invalid					

If the OS pins are set to select an OS ratio of eight, the next CONVST x rising edge takes the first sample for each channel, and the remaining seven samples for all channels are taken with an internally generated sampling signal. These samples are then averaged to yield an improvement in SNR performance. Table 1 shows typical SNR performance for both the ±10 V and the ±5 V range. As Table 8 shows, there is an improvement in SNR as the OS ratio increases. As the OS ratio increases, the 3 dB frequency is reduced, and the allowed sampling frequency is also reduced. In an application where the required sampling frequency is 10 kSPS, an OS ratio of up to 16 can be used. In this case, the application sees an improvement in SNR, but the input 3 dB bandwidth is limited to ~6kHz.The CONVST A and CONVST B pins must be tied/driven together when oversampling is turned on. When the over- sampling function is turned on, the BUSY high time for the conversion process extends. The actual BUSY high time depends on the oversampling rate that is selected: the higher the oversampling rate, the longer the BUSY high, or total conversion time (see Table 4).

Figure 19 shows that the conversion time extends as the over- sampling rate is increased, and the BUSY signal lengthens for the different oversampling rates. For example, a sampling frequency of 10 kSPS yields a cycle time of 100 µs. Figure 47 shows OS × 2 and OS × 4; for a 10 kSPS example, there is adequate cycle time to further increase the oversampling rate and yield greater improvements in SNR performance. In an application where the initial sampling or throughput rate is at 200 kSPS, for example, and oversampling is turned on, the throughput rate must be reduced to accommodate the longer conversion time and to allow for the read. To achieve the fastest throughput rate possible when over-sampling is turned on, the read can be performed during the BUSY high time. The falling edge of BUSY is used to update the output data registers with the new conversion data; therefore, the reading of conversion data should not occur on this edge.

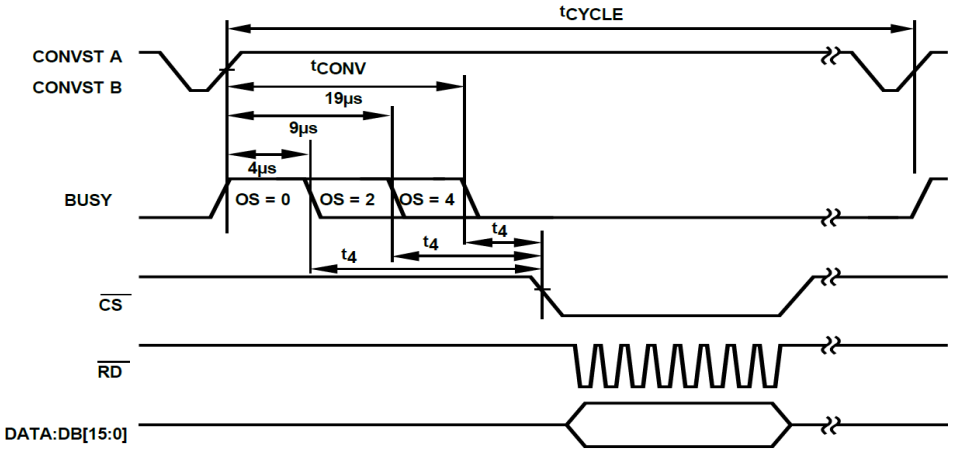


Figure 19. No Oversampling, Oversampling × 2, and Oversampling × 4 While Using Read After Conversion.

Figure 20 to Figure 26 illustrate the effect of oversampling on the code spread in a dc histogram plot. As the oversample rate is increased, the spread of the codes is reduced.When the oversampling mode is selected for the ADCS8162, it has the effect of adding a digital filter function after the ADC. The different oversampling rates and the CONVST sampling frequency produce different digital filter frequency profiles.

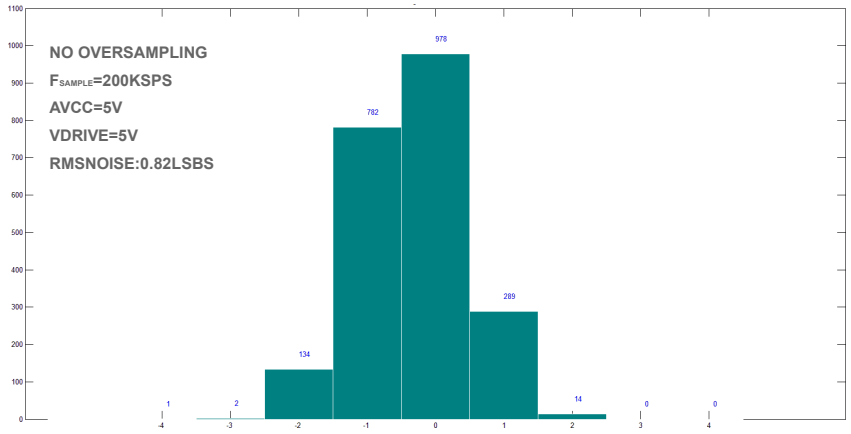


Figure 20. Histogram of Codes—No OS

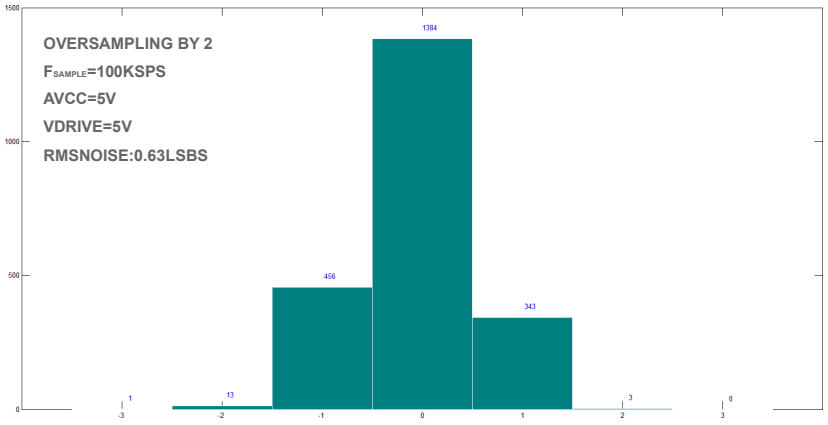


Figure 21. Histogram of Codes—OS ×2

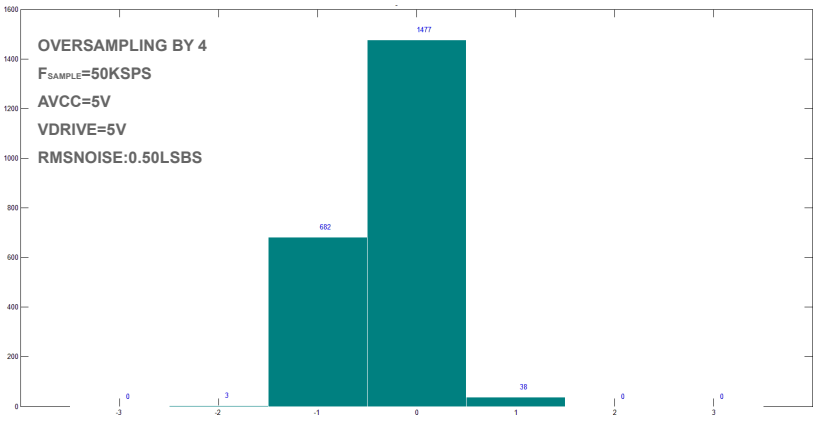


Figure 22. Histogram of Codes—OS ×4

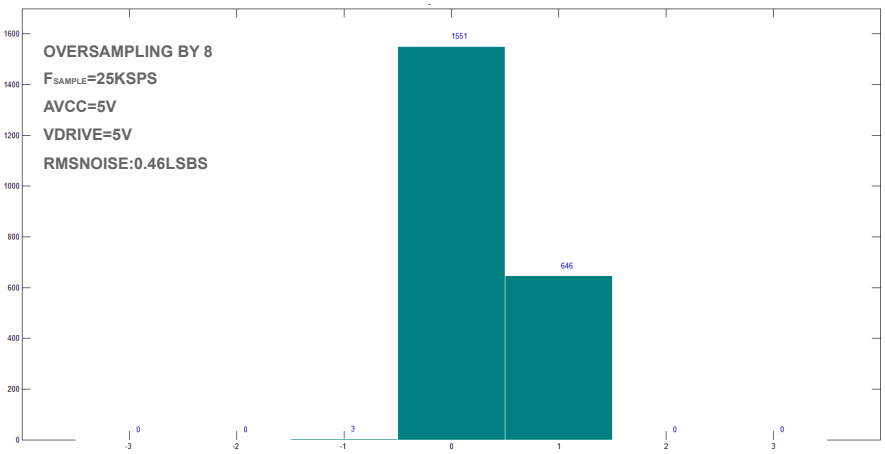


Figure 23. Histogram of Codes—OS × 8

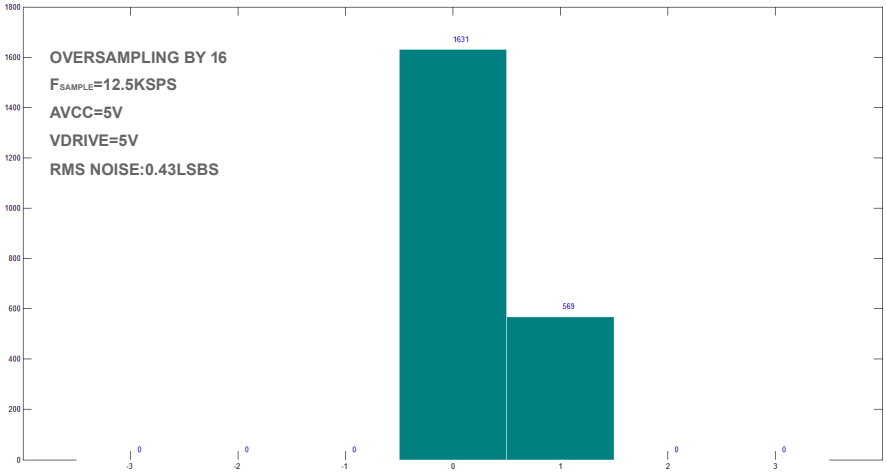


Figure 24. Histogram of Codes—OS ×16

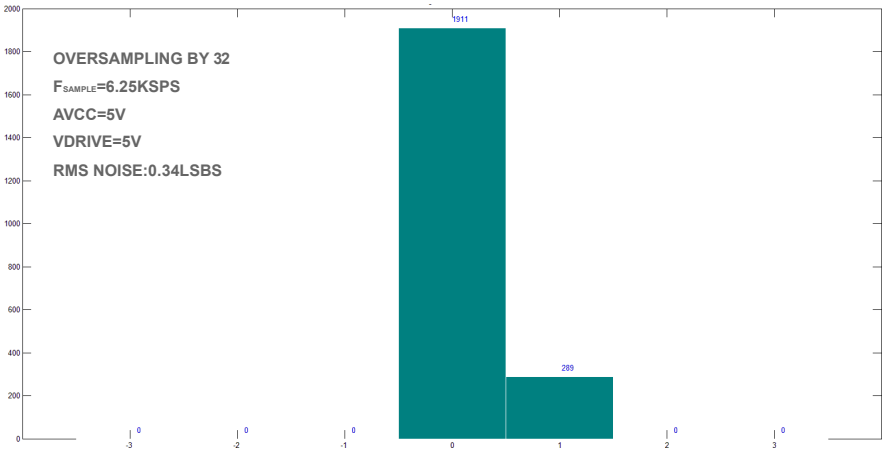


Figure 25. Histogram of Codes—OS ×32

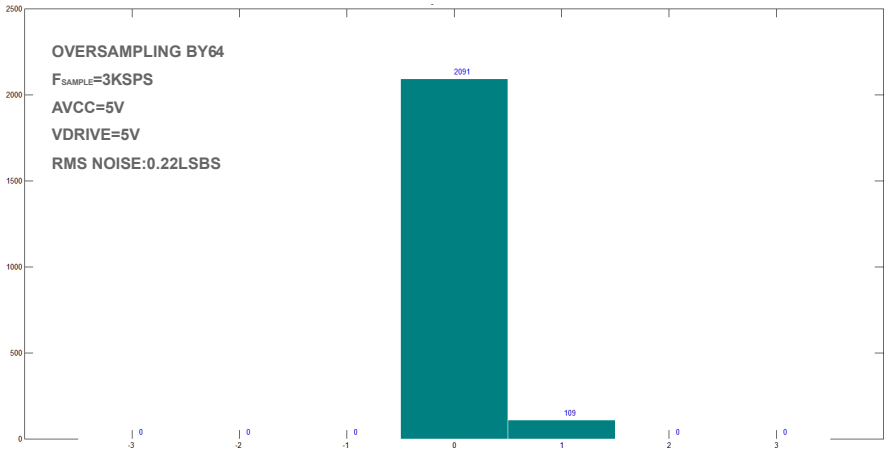


Figure 26. Histogram of Codes—OS × 64

11.PCBLAYOUT GUIDELINES

The printed circuit board that houses the ADCS8162 should be designed so that the analog and digital sections are separated and confined to different areas of the board.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the case of the split plane, the digital and analog ground planes should be joined in only one place, preferably as close as possible to the ADCS8162.

If the ADCS8162 are in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point: a star ground point that should be established as close as possible to the ADCS8162. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. The analog ground plane should be allowed to run under the ADCS8162 to avoid noise coupling. Fast switching signals like CONVST A, CONVST B, or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Avoid crossover of digital and analog signals. Traces on layers in close proximity on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the AVCC and VDRIVE pins on the ADCS8162 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Where possible, use supply planes and make good connections between the ADCS8162 supply pins and the power tracks on the board. Use a single via or multiple vias for each supply pin.

Good decoupling is also important to lower the supply impedance presented to the ADCS8162 and to reduce the magnitude of the supply spikes. The decoupling capacitors should be placed close to (ideally, right up against) these pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA and REFCAPB pins as close as possible to their respective ADCS8162 pins; and, where possible, they should be placed on the same side of the board as the ADCS8162 device.

Figure 27 shows the recommended decoupling on the top layer of the ADCS8162 board. Figure 28 shows bottom layer decoupling, which is used for the four AVCC pins and the VDRIVE pin decoupling. Where the ceramic 100 nF caps for the AVCC pins are placed close to their respective device pins, a single 100 nF capacitor can be shared between Pin 37 and Pin 38.

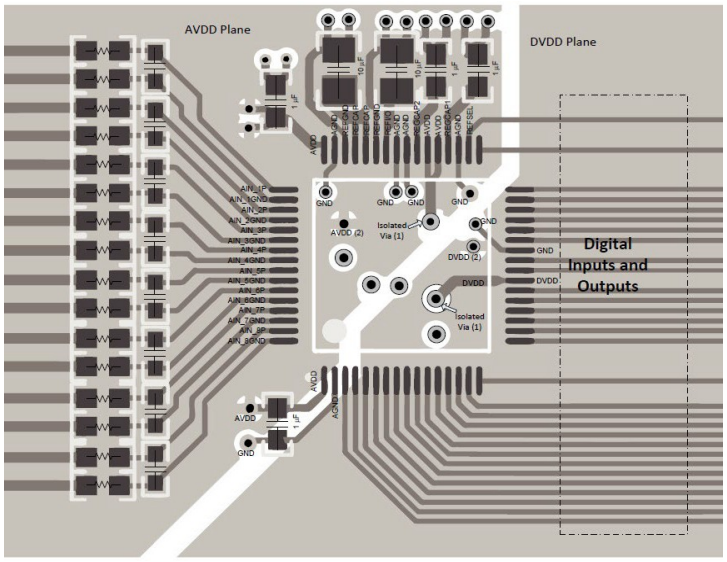


Figure 27. Top Layer Layout for all pin

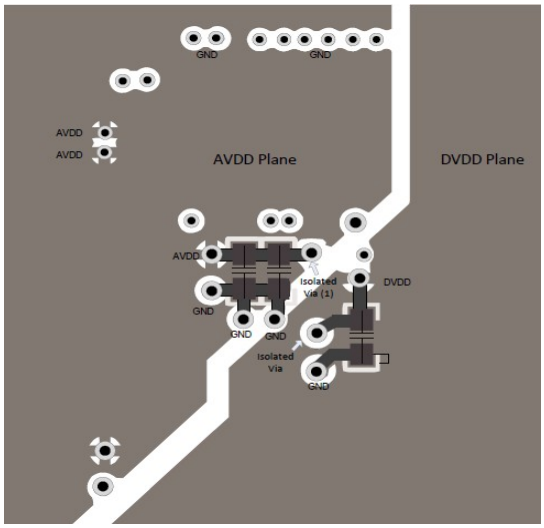


Figure 28. Bottom Layer Layout

To ensure good device-to-device performance matching in a system that contains multiple ADCS8162 devices, a symmetrical layout between the ADCS8162 devices is important.
Figure 29 shows a layout with two ADCS8162 devices. The AVCC supply plane runs to the right of both devices, and the VDRIVE supply track runs to the left of the two devices. The reference chip is positioned between the two devices, and the reference voltage track runs north to Pin 42 of U1 and south to Pin 42 of U2. A solid ground plane is used.
These symmetrical layout principles can also be applied to a system that contains more than two ADCS8162 devices. The ADCS8162 devices can be placed in a north-south direction, with the reference voltage located midway between the devices and the reference track running in the north-south direction, similar to Figure 59.

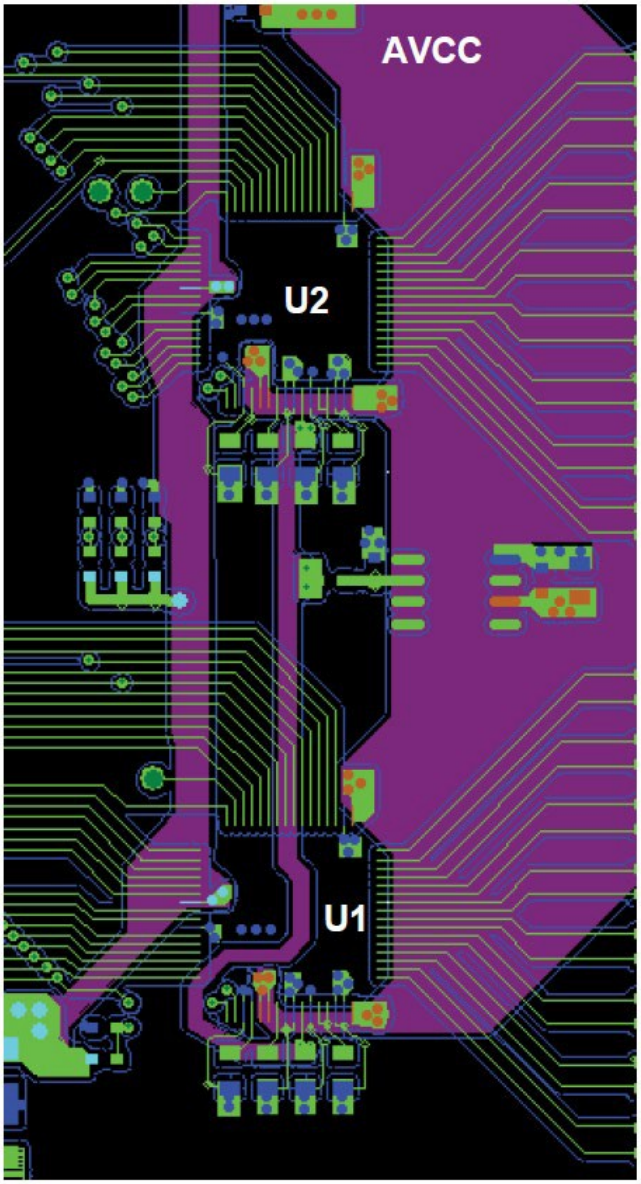
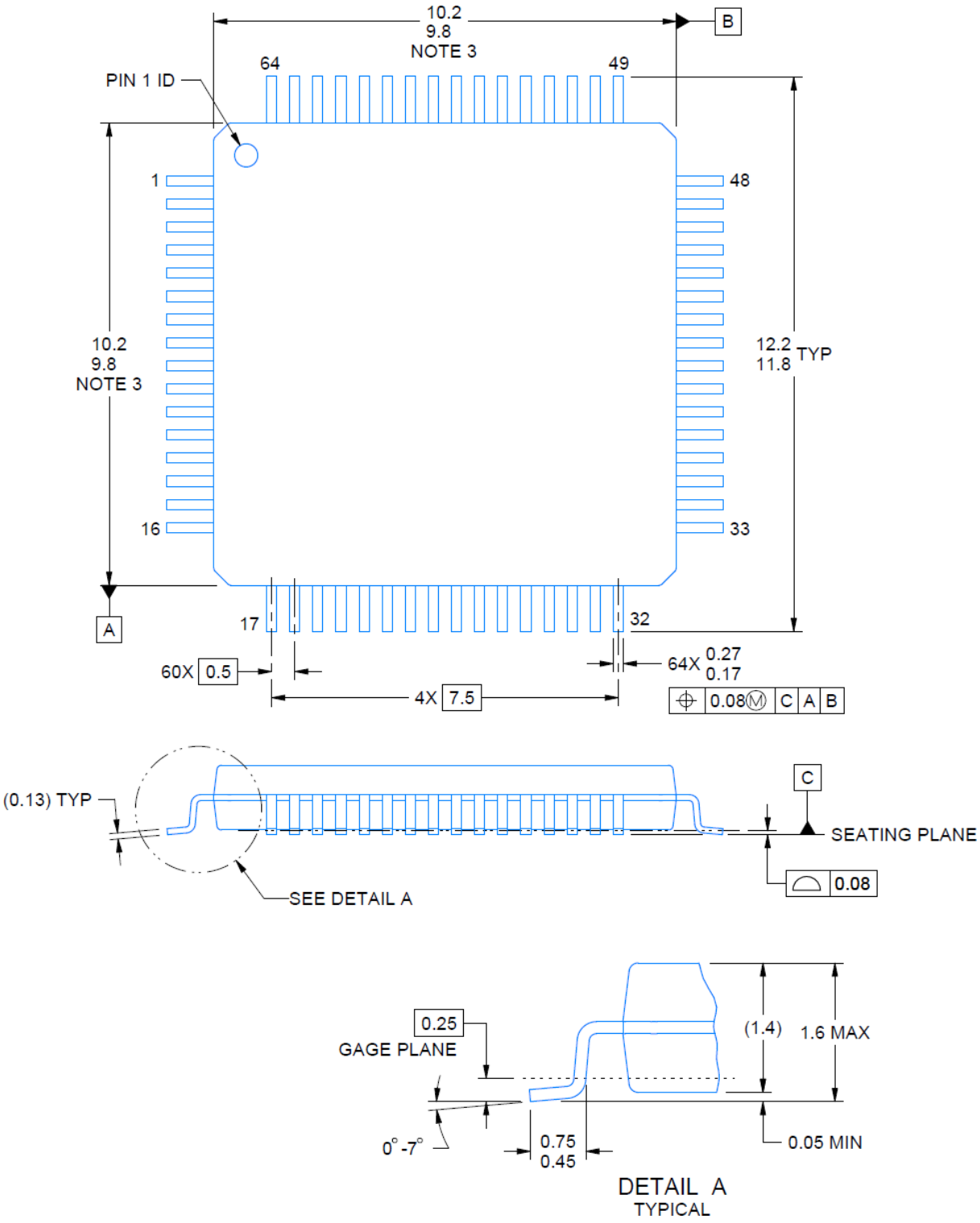
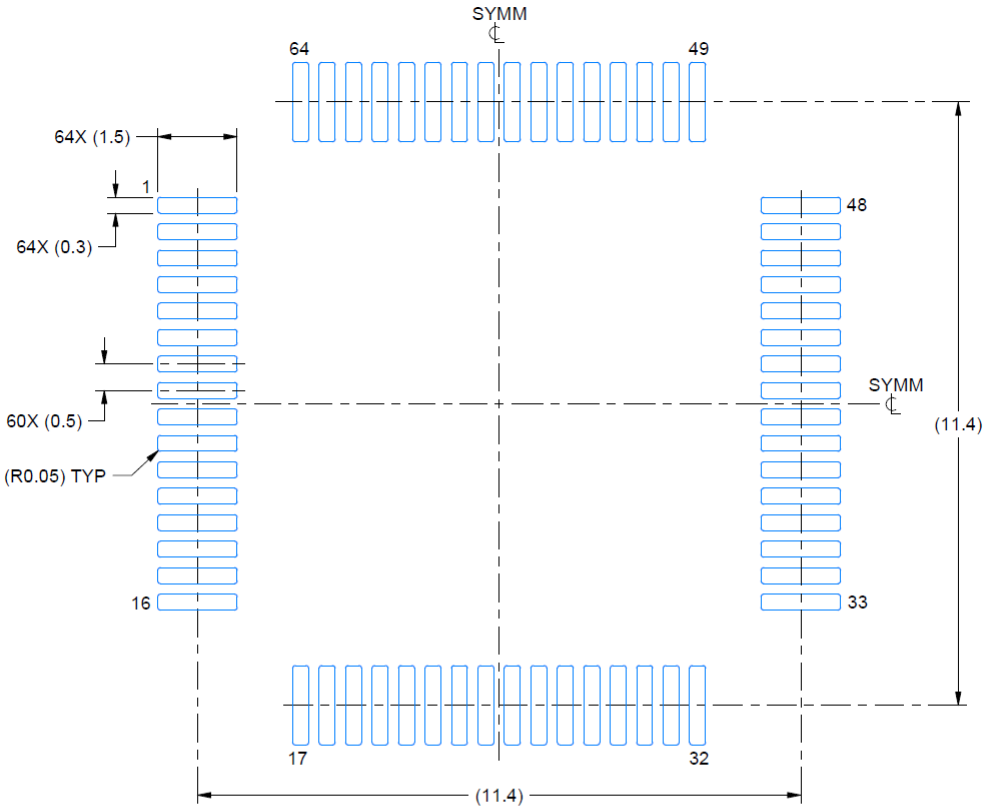


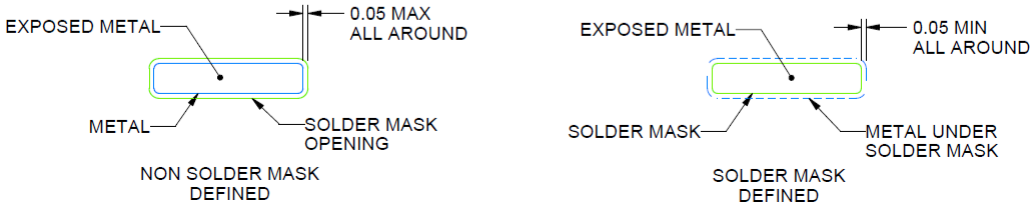
Figure 29. Layout for Multiple ADCS8162 Devices—Top Layer and Supply Plane Layer

11.1OUTLINE DIMENSIONS





LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



11.2 Ordering Information

Product Code	Temperature Code	Package Code	Packing Form
ADCS8162LFP	A	64-LQFP	1280/REEL
ADCS8162MLFP	B	64-LQFP	1280/REEL

Notes1:

Temperature Code Definition: A for -40℃ to 85℃; B for -40℃ to 125℃; C for -40℃ to 150℃

Package Form Definition: Reel for tape and real; BP for bulk packaging